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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,826	08/05/2004	Stephen W. Bedell	FIS920040069	4825

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EXAMINER	
DOTY, HEATHER ANNE	

ART UNIT	PAPER NUMBER
2813	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,826	BEDELL ET AL.	
	Examiner	Art Unit	
	Heather A. Doty	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 30 January 2006.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-3 and 6-19 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-3 and 6-19 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 24 October 2005 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless – (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 8-11, 13-16, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Wang et al. (*SiGe band engineering for MOS, CMOS and quantum effect devices*, Journal of Materials Science: Materials in Electronics **6** (1995) 311-324).

Regarding claim 8, Wang et al. teaches a method of fabricating a semiconductor device, comprising the steps of:

forming a layer of a digital alloy of SiGe on a substrate (p. 322, Fig. 14(a)); and

forming a Si layer on the digital alloy of SiGe (p. 322, Fig. 14(a)), wherein the substrate is a silicon-on-insulator (SOI) structure of a SiGe-on-insulator (SGOI) structure (p. 322, paragraph bridging columns 1 and 2 teaches that a SUPERFET, such as the one illustrated in Fig 14, can be studied on SOI substrates), and the digital alloy of SiGe has a thermal conductivity greater than that of a random alloy of Si and Ge (paragraph 0022 of the instant specification discloses that a superlattice of alternating Si and Ge layers, wherein each layer contains only one element, such as the one taught in Wang et al., has a thermal conductivity greater than that of a random allow of Si and Ge).

Regarding claim 9, Wang et al. teaches a method according to claim 8, wherein the digital alloy layer is characterized as a relaxed SiGe layer, and said Si layer is a

strained Si layer (paragraph 0025 of the instant specification discloses that in a digital alloy multilayer of Si and Ge, such as the one taught by Wang et al., the individual Si and Ge layers will have stress due to the lattice mismatch with the layer below, but the combined layer has effectively zero stress, and a Si layer grown on top of the combined layer will be strained).

Regarding claim 10, Wang et al. teaches the method according to claim 8, wherein the digital alloy layer includes a plurality of alternating sublayers of Si and Ge (p. 322, Fig. 14(a)).

Regarding claim 11, Churchill et al. teaches the method according to claim 10, wherein the sublayers are formed with thicknesses in accordance with a desired composition ratio of the digital alloy of SiGe (p. 321, second full paragraph).

Regarding claim 13, Wang et al. teaches a semiconductor device comprising a layer of a digital alloy of SiGe on a substrate; and a Si layer on the digital alloy of SiGe (p. 322, Fig. 14(a)), wherein the substrate is a silicon-on-insulator (SOI) structure of a SiGe-on-insulator (SGOI) structure (p. 322, paragraph bridging columns 1 and 2 teaches that a SUPERFET, such as the one illustrated in Fig 14, can be studied on SOI substrates), and the digital alloy of SiGe has a thermal conductivity greater than that of a random alloy of Si and Ge (paragraph 0022 of the instant specification discloses that a superlattice of alternating Si and Ge layers, wherein each layer contains only one element, like the one taught in Wang et al., has a thermal conductivity greater than that of a random allow of Si and Ge).

Regarding claim 14, Wang et al. teaches a device according to claim 13, wherein the digital alloy layer is characterized as a relaxed SiGe layer, and said Si layer is a strained Si layer (paragraph 0025 of the instant specification discloses that in a digital alloy multilayer of Si and Ge, such as the one taught by Wang et al., the individual Si and Ge layers will have stress due to the lattice mismatch with the layer below, but the combined layer has effectively zero stress, and a Si layer grown on top of the combined layer will be strained).

Regarding claim 15, Wang et al. teaches the device according to claim 13, wherein the digital layer comprises a plurality of alternating sublayers of Si and Ge (pg. 322, Fig. 14(a)).

Regarding claim 16, Wang et al. teaches the device according to claim 15, wherein the sublayers are formed with thicknesses in accordance with a desired composition ratio of the digital alloy of Si Ge (p. 321, second full paragraph).

Regarding claim 19, Wang et al. teaches the device according to claim 15, and further teaches that a sublayer of Si is disposed on the substrate (p. 322, Fig. 14(a) shows the Si/Ge superlattice in the channel region of a CMOS device with a sublayer of n- or p-type Si on the substrate.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 12 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (*SiGe band engineering for MOS, CMOS and quantum effect devices*, Journal of Materials Science: Materials in Electronics **6** (1995) 311-324) in view of Fukuda et al. (U.S. 2004/0004271).

Regarding claims 12 and 17, Wang et al. teaches the method according to claim 10 and the device according to claim 15 (note 35 U.S.C. 102(b) rejection above), but does not teach that at least one of the first layer and the second layer, or that each of the sublayers, consists essentially of a single isotope.

However, Fukuda et al. teaches that the thermal conductivity of Si or Ge crystals increases when the crystals consist essentially of a single isotope of Si or Ge (paragraphs 0101-0113).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method or make the device taught by Wang et al., and further form at least one of the first layer and the second layer, or each of the sublayers, so that they consist essentially of a single isotope. The motivation for doing so at the time of the invention would have been to increase the thermal conductivity of the layers, as expressly taught by Fukuda et al.

Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Churchill et al. (*Optical etalon effects and electronic structure in silicon-germanium 4 monolayer: 4 monolayer strained layer superlattices*, Semicond. Sci. Technol. **6** (1991) 18-26) in view of Wang et al. (*SiGe band engineering for MOS, CMOS and quantum effect devices*, Journal of Materials Science: Materials in Electronics **6** (1995) 311-324).

Regarding claim 1, Churchill et al. teaches a method of forming a SiGe layer on a substrate, the method comprising the steps of:

depositing a first layer of one of Si and Ge in a first depositing step on said substrate (abstract; p. 2, section 2.1);

depositing a second layer of the other of Si and Ge on the first layer in a second depositing step (abstract; p. 2, section 2.1); and

repeating said first depositing step and said second depositing step so as to form a combined SiGe layer having a plurality of Si layers and a plurality of Ge layers, wherein respective thicknesses of the Si layers and Ge layers are in accordance with a desired composition ratio of the combined SiGe layer (p. 18, second paragraph discloses the desired composition ratio given by 4:4 monolayers Si: monolayers Ge), and the combined SiGe layer is characterized as a digital alloy of Si and Ge having a thermal conductivity greater than that of a random alloy of Si and Ge (paragraph 0022 of the instant specification discloses that a superlattice of alternating Si and Ge layers, wherein each layer contains only one element, such as the one taught in Churchill et al., has a thermal conductivity greater than that of a random allow of Si and Ge).

Churchill et al. does not teach that the substrate is a silicon-on-insulator (SOI) structure or a SiGe-on-insulator (SGOI) structure.

Wang et al. teaches the advantages of using Si/Ge superlattices as channel material for FETs. Such structures offer high mobility (p. 321, column 2, paragraph 2). Wang et al. additionally teaches the advantages of forming such structures on SOI substrates (p. 322, paragraph bridging columns 1 and 2). Among other advantages,

Wang et al. teaches that SOI substrates allow for isolation of n- and p-channel devices without the use of p-n junctions (p. 319, third full paragraph).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Churchill et al. to grow a Si/Ge superlattice structure on a substrate, and further grow the structure on an SOI substrate, since Wang et al. teaches the advantages both of incorporating a Si/Ge superlattice structure into a FET device, and of forming such a device on an SOI substrate.

Regarding claim 3, Churchill et al. and Wang et al. together teach the method according to claim 1. Churchill et al. further teaches the step of depositing a Si layer on the combined SiGe layer, wherein the combined SiGe layer is further characterized as a relaxed SiGe layer, and said Si layer is a strained Si layer (p. 19, lines 1-3 of section 2.1; paragraph 0025 of the instant specification discloses that in a digital alloy multilayer of Si and Ge, such as the one taught by Churchill et al., the individual Si and Ge layers will have stress due to the lattice mismatch with the layer below, but the combined layer has effectively zero stress, and a Si layer grown on top of the combined layer will be strained).

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Churchill et al. (*Optical etalon effects and electronic structure in silicon-germanium 4 monolayer: 4 monolayer strained layer superlattices*, Semicond. Sci. Technol. **6** (1991) 18-26) in view of Wang et al. (*SiGe band engineering for MOS, CMOS and quantum effect*

devices, Journal of Materials Science: Materials in Electronics **6** (1995) 311-324), as applied to claim 1 above, and further in view of Fukuda et al. (U.S. 2004/0004271).

Regarding claim 7, Churchill et al. and Wang et al. together teach the method according to claim 1, but do not teach that at least one of the first layer and the second layer, or that each of the sublayers, consists essentially of a single isotope.

However, Fukuda et al. teaches that the thermal conductivity of Si or Ge crystals increases when the crystals consist essentially of a single isotope of Si or Ge (paragraphs 0101-0113).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Churchill et al. and Wang et al. together, and further form at least one of the first layer and the second layer, or each of the sublayers, so that they consist essentially of a single isotope. The motivation for doing so at the time of the invention would have been to increase the thermal conductivity of the layers, as expressly taught by Fukuda et al.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Churchill et al. (*Optical etalon effects and electronic structure in silicon-germanium 4 monolayer: 4 monolayer strained layer superlattices*, Semicond. Sci. Technol. **6** (1991) 18-26) in view of Wang et al. (*SiGe band engineering for MOS, CMOS and quantum effect devices*, Journal of Materials Science: Materials in Electronics **6** (1995) 311-324), as applied to claim 1 above, and further in view of Werner et al. (U.S. 2004/0140531).

Regarding claim 2, Churchill et al. and Wang et al. together teach the method of claim 1, but do not teach that one or more of the Ge layers has a thickness of about 10 Å.

Werner et al. teaches a Si/Ge superlattice wherein the Ge layers have a thickness of 90 nm, which is 9 Å , which is about 10 Å (paragraph 0050). Moreover, it has been held that "where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller* 105 USPQ233, 255 (CCPA 1955).

Therefore, at the time of the invention, it would have been obvious to use the method taught by Churchill et al. and Wang et al. together, and further optimize the thickness of one or more of the Ge layers to arrive at around 10 Å, as taught by Werner.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (*SiGe band engineering for MOS, CMOS and quantum effect devices*, Journal of Materials Science: Materials in Electronics **6** (1995) 311-324) in view of Werner et al. (U.S. 2004/0140531).

Regarding claim 18, Wang et al. teaches the device of claim 15, but does not teach that one or more of the Ge layers has a thickness of about 10 Å.

Werner et al. teaches a Si/Ge superlattice wherein the Ge layers have a thickness of 90 nm, which is 9 Å , which is about 10 Å (paragraph 0050). Moreover, it has been held that "where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller* 105 USPQ233, 255 (CCPA 1955).

Therefore, at the time of the invention, it would have been obvious to make the device taught by Wang et al., and further optimize the thickness of one or more of the Ge layers to arrive at around 10 Å, as taught by Werner.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Churchill et al. (*Optical etalon effects and electronic structure in silicon-germanium 4 monolayer: 4 monolayer strained layer superlattices*, Semicond. Sci. Technol. **6** (1991) 18-26) in view of Wang et al. (*SiGe band engineering for MOS, CMOS and quantum effect devices*, as applied to claim 1 above, and further in view of Lee et al. (U.S. 5,665,631).

Regarding claim 6, Churchill et al. and Wang et al. together teach the method of claim 1, but do not teach that the substrate has an upper layer, or polishing said upper layer to reduce the thickness thereof before the first depositing step.

Lee et al. teaches a method of forming a conventional SOI substrate (Figs. 1A and 1B; column 1, line 53 – column 2, line 7). The last step of the process is to polish the upper layer to thin it to a desired thickness (column 2, lines 1-7).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Churchill et al. and Wang et al. together, and further polish the upper layer of the SOI substrate to reduce the thickness thereof, before the first depositing step, as taught by Lee et al. to be conventional processing in the manufacture of SOI substrates.

Response to Arguments

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

had

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